RS6563

High Performance PFC Controller

General Description

RS6563 is an active power factor correction (PFC) controller for AC/ DC switching mode power supply applications. It is designed for operating in critical conduction mode (CRM).

RS6563 features a quadrant multiplier. It includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even a large load range. RS6563 also features an internal start-up time for stand-alone applications, Zero Current Detector (ZCD), peak current sense comparator, and a totem pole output.

RS6563 ensures safe operation with complete protections against all the fault conditions. Built-in protection circuitry includes system over voltage protection (OVP), VCC under voltage lockout (UVLO), cycle-by-cycle current limiting, multiplier output clamping for limiting maximum peak switch current, system open loop protection, and gate drive output clamping for external power MOSFET protection.
In RS6563, a two-step OVP which contains dynamic OVP and static OVP enables to safely handle over voltage either occurring at start-up or resulting from load disconnection.

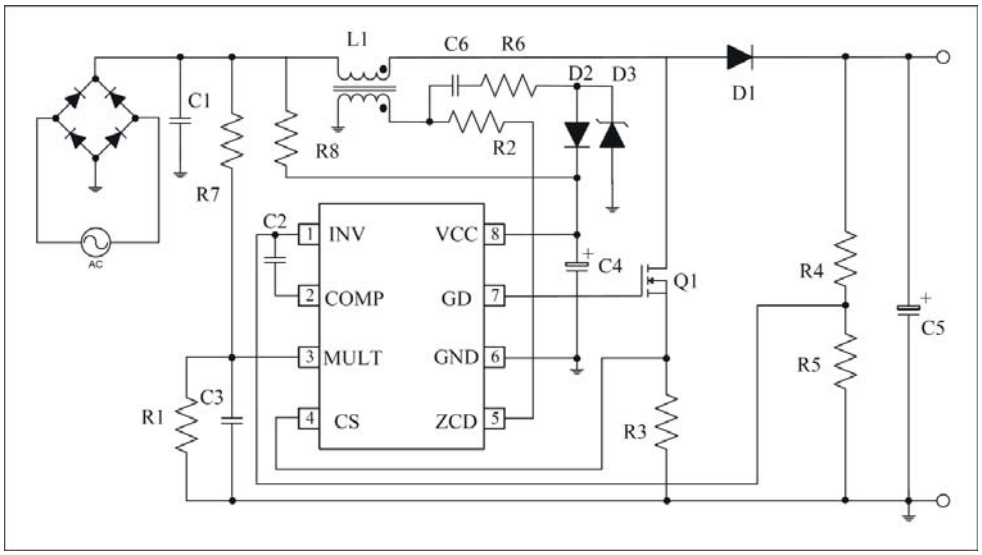
Features

- Active transition-mode(TM) optimizer
- One quadrant multiplier with THD optimizer
- Low dynamic OVP sensing current setting
- Low start-up current and operating current
- Cycle-by-Cycle current limiting
- Internal RC filter
- Trimmed 1.5% internal band-gap reference
- Under Voltage Lockout (UVLO) with Hysteretic
- Dynamic and static output over-voltage protection
- Internal start-up timer for stand-alone clamping
- Disable function
- Totem pole output with high state clamping
- System open loop protection
- Proprietary Audio Noise Free Operation
- 9.5V to 30V wide range of V_{CC} voltage
- DIP-8 & SOP-8 package
- RoHS Compliant and 100% Lead (Pb)-Free and Green (Halogen Free with Commercial Standard)

Applications

- Electronic Ballast
- AC/DC SMPS power supply

Application Circuits



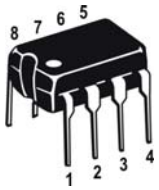
This integrated circuit can be damaged by ESD. Orister Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Pin Assignments

SOP-8

DIP-8

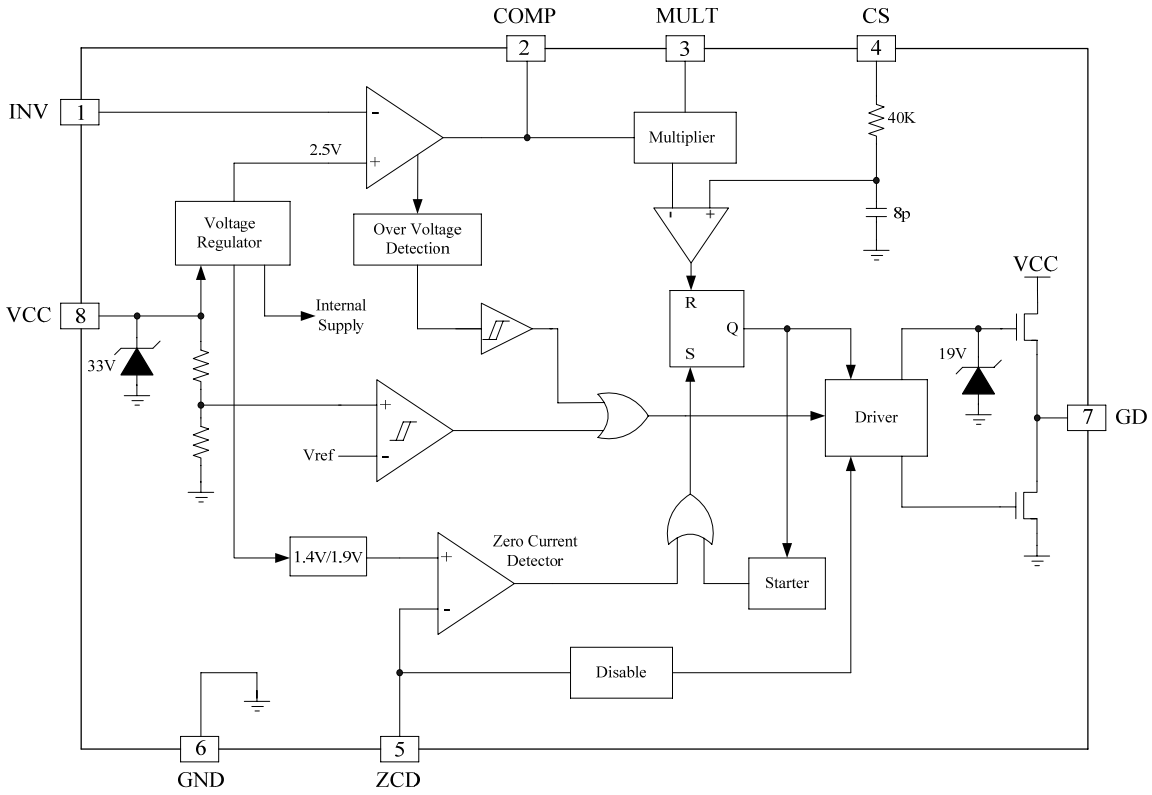


PACKAGE	PIN	SYMBOL	DESCRIPTION
SOP-8/DIP-8	1	INV	Inverting Input of Error Amplifier. Connected to Resistor Divider from system Output. This is also used for system open loop protection.
	2	COMP	Out of Error Amplifier. A feedback compensation network is placed between COMP and the INV pin.
	3	MULT	Input of Multiplier. Connected to Line Voltage after Bridge Diodes via A Resistor Divider to provide Sinusoidal Reference Voltage to the Current loop.
	4	CS	Current Sense Input pin. Connected to MOSFET Current Sensing Node.
	5	ZCD	Zero Current Detection Input. When Activated, A New Switching Cycle Starts. If it is connected to GND, the device is disabled.
	6	GND	Ground pin
	7	GD	Gate driver output. Drive power MOSFET.
	8	VCC	DC Power Supply Voltage.

Ordering Information

DEVICE	DEVICE CODE
RS6563 Y Z	**Y** is package & Pin Assignments designator : S : SOP-8 P ： DIP-8 **Z** is Lead Free designator : P: Commercial Standard, Lead (Pb) Free and Phosphorous (P) Free Package G: Green (Halogen Free with Commercial Standard)

Block Diagram



Absolute Maximum Ratings

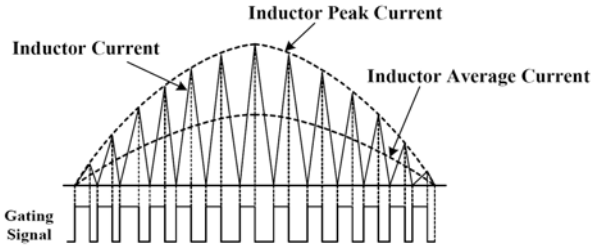
SYMBOL	PARAMETER	RANGE	UNITS
V_{CC}	DC Supply voltage	30	V
I_{ZCD}	Zero Current Detector Max. Current	50mA (source), -10mA (sink)	mA
C_S INV COMP MULT	Analog inputs & outputs	-0.3 to 7.0	V
T_J	Min/Max operating Junction Temperature	-40 to 150	°C
T_{SGT}	Min/Max storage temperature	-55 to 150	°C
Lead Temperature	(Soldering, 10secs)	260	°C

Electrical Characteristics (T_A=25°C, unless otherwise specified)

SYMBOL	PIN	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE SECTION							
Vcc	8	Operating Range	After Turn On	11	-	30	V
UVLO	8	Turn-on threshold	-	11	12	13	V
	8	Turn-off threshold	-	8.5	9.5	10.5	V
Hys	8	Hysterics	-	-	2.5	-	V
Vz	8	Zener voltage	Icc=5mA	30	33	36	V
SUPPLY CURRENT SECTION							
$I_{CC-START}$	8	Start-up Current	V_{CC}=11V	-	35	70	uA
I_Q	8	Quiescent Current, No switching	V_{CC}=14.5V	-	3	4	mA
I_{CC}	8	Operating Supply Current	C_L=1nF@70KHz	-	4	5.5	mA
			In OVP condition Vpin1=2.7V	-	1.4	2.1	mA
I_Q	8	Quiescent Current	Vpin5≤150mV, V_{CC}=14.5V	-	1.1	2.1	mA
			Vpin5≤150mV, V_{CC}<V_{CC} off	-	35	70	μA
ERROR AMPLIEIER SECTION							
V_{INV}	1	Voltage Feed- back input threshold	V_{CC}=14.5V	2.45	2.5	2.55	V
V_{INV}	1	Line Regulation	12V<V_{CC}<28V	-	2	5	mV
I_{INV}	1	Input Bias Current	I_{DD}=10mA	-	-0.1	-1	μA
Gv		Voltage Gain	Open loop	60	80	-	dB
Gd		Gain Bandwidth	-	-	1.2		MHz
Icomp	2	Source Current	V_{COMP}=3.6V, V_{INV}=2.4V	-2	-6	10	mA
		Sin Current	V_{COMP}=3.6V, V_{INV}=2.6V	2	6	10	mA
Vcomp	2	Upper clamp voltage	I_{SOURCE}=0.5mA	-	5.2	-	V
		Lower clamp voltage	I_{SINK}=0.2mA	-	2.25	-	V
MULTIPLIER SECTION							
Vmult	3	Linear Operating Range	V_{COMP}=3.0V	0	-	3.5	V
ΔV_{CS}/ ΔVmult		Output Max. slope	Vmult=from 0 to 0.5V V_{COMP}=Upper clamp Voltage	1.65	1.9	-	V/V
K		Gain	Vmult=1V, V_{COMP}=3.5V	0.5	0.65	0.8	1/V
CURRENT SENSE COMPARATOR							
V_{CS}	4	Current Sense Reference Clamp	Vmult=2.5V V_{COMP}=Upper Clamp Voltage	1.6	1.7	1.8	V
I_{CS}	4	Input bias Current	V_{CS}=0	-	-	0.1	uA
$T_{D(H-L)}$	4	Delay to output	-	-	200	450	nS
ZERO CURRENT DETECTOR							
Vzcd	5	Input Threshold Voltage Rising Edge	-	-	1.9	-	V
		Hysteretic	-	0.3	0.5	0.7	V
Vzcd	5	Upper Clamp voltage	Izcd=2.5mA	5.1	5.7	6.3	V
Vzcd	5	Lower Clamp voltage	Izcd=-2.5mA	0.4	0.65	0.8	V
Izcd	5	Input Bias Current	1.0V≤Vzcd≤4.5V	-	2	-	μA
Izcd	5	Source Current Capability	-	-3	-	-5	mA
Izcd	5	Sink Current After Disable	-	3	-	10	mA
Vdis	5	Disable threshold	-	150	250	350	mV
Izcd	5	Restart Current after Disable	Vzcd<Vides, Vcc>Vccoff	-100	-200	-400	μA
GATE DRIVE SECTION							
V_{OL}	7	Low output voltage	V_{CC}=14.5V, I_O=100mA	-	-	1.5	V
V_{OH}	7	High output voltage	V_{CC}=14.5V, I_O=100mA	8	-	-	V
T_R	7	Rising Time	C1=1000pf,10 to 90%	-	80	150	ns
T_F	7	Falling Time	C1=1000Pf,10 to 90%	-	30	70	ns
V_{OCLAMP}	7	Output Clamp Voltage	V_{CC}=28V	-	16	18	V
OUTPUT OVER VOLTAGE SECTION							
I_{OVP}	2	Dynamic OVP Triggering Current	-	-	40	-	μs
-	-	Static OVP Threshold	-	-	2.3	-	V
STARTUP TIMER							
T_{START}	-	Re-start timer period	-	70	150	300	μs
SYSTEM OPEN LOOP PROTECTION COMPARATOR							
V_{TH-OL}	-	System Open loop protection comparator Threshold	-	-	250	-	mV

Operation Description

RS6563 is a highly integrated power factor correction (PFC) controller IC that operates in critical conduction mode (CRM). It turns on MOSFET when the inductor current reaches zero and turns off MOSFET when the inductor current meets the desired input current reference voltage as shown below.



Inductor Current Waveform

In this way, the input current waveform follows that the input voltage, therefore a good factor is obtained.

Startup Operation

VDD is the power supply terminal for the RS6563. The startup resistor from the rectified high voltage DC rail supplies current to the VDD bypass capacitor. During startup, the RS6563 typically draws only lower than 70uA, so that VDD could be quickly charged up above UVLO threshold. A large value startup resistor can be used to minimize the power loss in standby mode. As soon as VDD is beyond the UVLO(OFF), the chip will begin to start.

Error Amplifier

The sensed and divided output voltage is feedback to the error amplifier inverting input (INV). This voltage is compared to an internal reference voltage (2.5V) to set the regulation on output voltage.

The EA output is internally connected to the multiplier input and externally connected for loop compensation. Generally, the system loop bandwidth is set below 20 Hz to suppress the AC ripple of the line voltage and get a good power factor. It is usually realized with a capacitor which connected between the inverting input and EA output.

Multiplier

The one quadrant multiplier output limits the MOSFET peak current with respect of the system output voltage and the AC half wave rectified input voltage. Through controlling the CS comparator threshold as the AC line voltage traverses sinusoidally from zero to peak line voltage, the PFC pre-regulator's load appears to be resistive to the AC line.

In RS6563, the two inputs for the multiplier are designed to achieve good linearity over a wide dynamic range to represent an AC line free from distortion. One is connected to an external resistor divider which monitors the rectified AC line voltage, the other one is internal driven by a DC voltage which is the difference between error amplifier output COMP and reference voltage, $V_{REF.}$

The equation (1) below describes the relationship between multiplier output and its inputs.

$$V_m = K \times V_{MULT} \times (V_{COMP} - Vref) \quad (1)$$

K : Multiplier Gain

V_{MULT} : Voltage at Pin 3(MULT)

V_{COMP} : Error Amplifier Output Voltage (COMP)

$Vref$: Internal 2.5V Reference Voltage

Zero Current Detection

RS6563 operates as a critical conduction mode controller. It can perform zero current detection by using an auxiliary winding of the inductor. When the stored energy is fully released to the output, the voltage at ZCD will decrease. Once the inductor current reaches ground level, the polarity of the voltage across the winding is reversed. When the ZCD input falls below 1.4V, the zero current detector will be triggered to turn on the power MOSFET and start a new switching cycle. To prevent false tripping, 0.5V hysteresis is provided. The zero current detector input is protected internal by two clamps. The upper 5.7V clamp prevents input over voltage breakdown while the lower 0.65V clamp prevents substrate injection.

Current Sensing

RS6563 detects primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the cycle-by-cycle current limit. The multiplier output voltage is compared with this sense voltage through an internal comparator to limit the inductor current. The maximum voltage threshold of the current sensing pin is set as 1.7V. Thus the MOSFET peak current can be calculated as:

$$I_{peak(\max)} = \frac{1.7V}{R_S} \qquad (2)$$

An internal RC filter is connected to the CS pin which smoothes the switch-on current spike. The remaining switch-on spike is blanked out via an internal leading edge blanking (LEB) circuit. Another extra function of LEB is that it limits the system minimum on time, thus the THD of system at light load will be decreased.

Protection Controls

A lot of good protections features have been implemented in RS6563 to prevent the power supply from being damaged caused by fault conditions. These protection features contains VCC under voltage lockout (UVLO), cycle-by-cycle current limiting, peak current limiting, output dynamic and static over-voltage protection (OVP), and output gate clamp.

Over Voltage Protection

Limited by low loop bandwidth setting, detection of output OVP could become very slow in regular approach. RS6563 offers two level OVP protection including dynamic OVP for output fast transient protection and static OVP for output stead-state protection.
In an output transient OVP event, currents in proportion to △V flows into Error Amplifier output COMP through compensation network. When this current reaches 32μA, the output of multiplier is forced to decrease and on-time of MOSFET is reduced. When current continues to exceed 40μA, the power MOSFET is turned off until the current falls below 10μA. In this way, the system output cannot reach to a very high value.

When OVP event lasts long enough, the Error Amplifier output, COMP, will saturate and stay low. Static OVP comparator is activated and power MOSFET Gate is off when COMP voltage is dropped below 2.30V. Normal operation is resumed when Error Amplifier goes back to its linear region after output voltage drops.

System open loop protection

RS6563 offers a function of system open loop protection. If INV pin is below 0.25V with 50mV hysteresis, the switching will turn off. In this way, the system output voltage cannot increase too high (only the rectified line voltage), and the pre-regulator will be protected from damage.

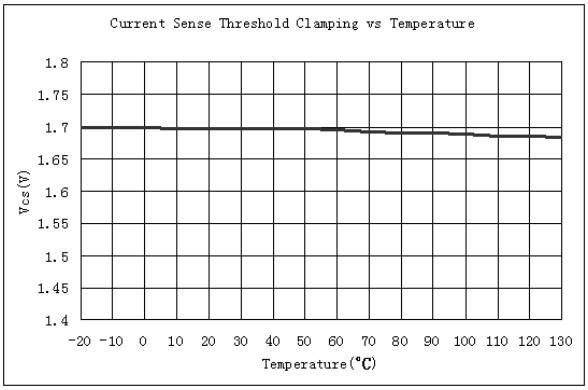
Disable function

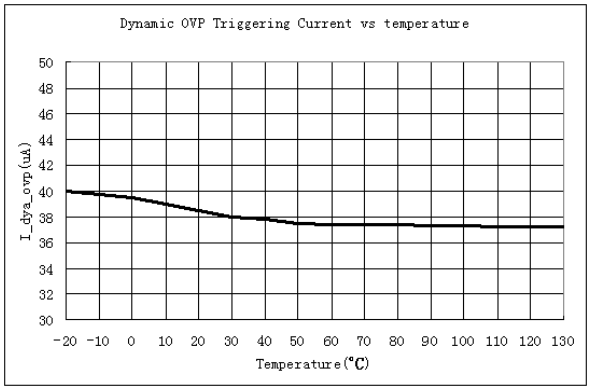
A disable function is provided in RS6563. When the ZCD pin is below 0.25V，RS6563 is disabled and some internal functional blocks are tuned off. The operation current is very small under this condition until the ZCD pin is released.

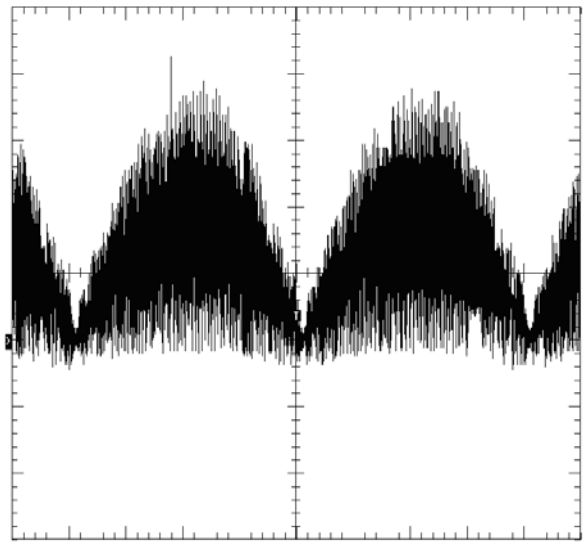
Gate Drive Output

RS6563 contains a singe totem-pole output stage designed specifically for a direct drive of power MOSFET. With a 1nF load, the rise time of the drive output is 80ns and the fall time is 30ns. The built-in 16V clamp at the gate output protects the MOSFET gate from high voltage stress.

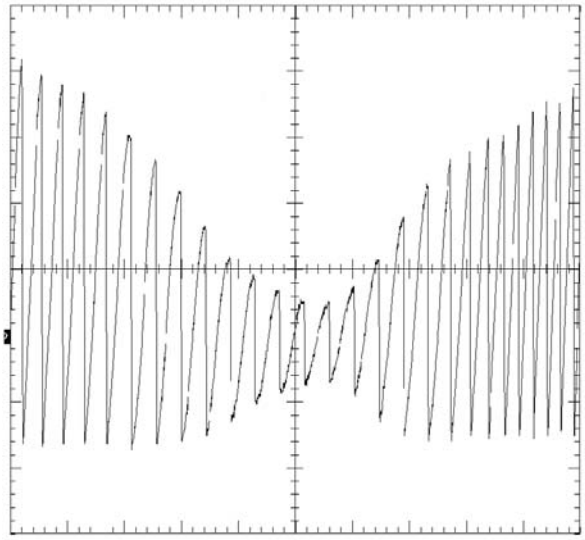
Typical Performance Characteristics



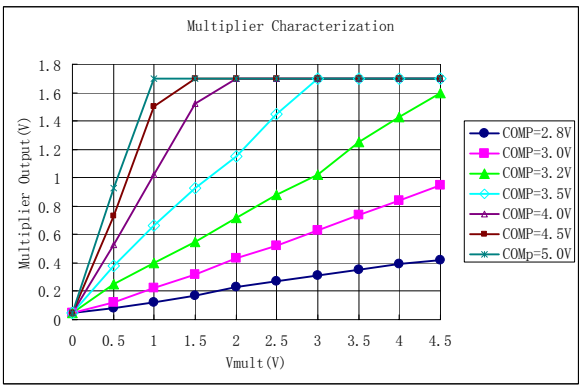




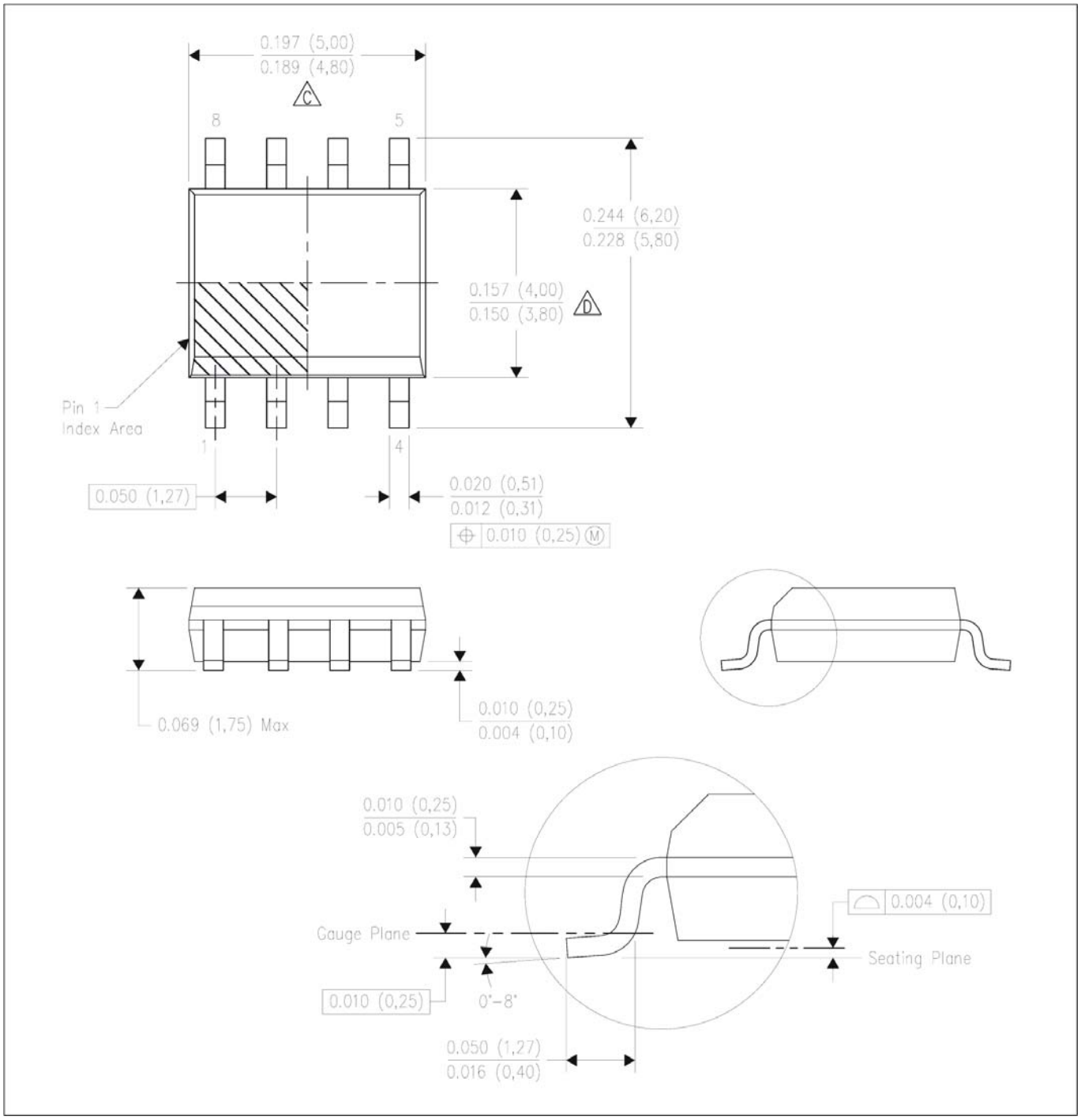
Inductor Current



THD Optimization



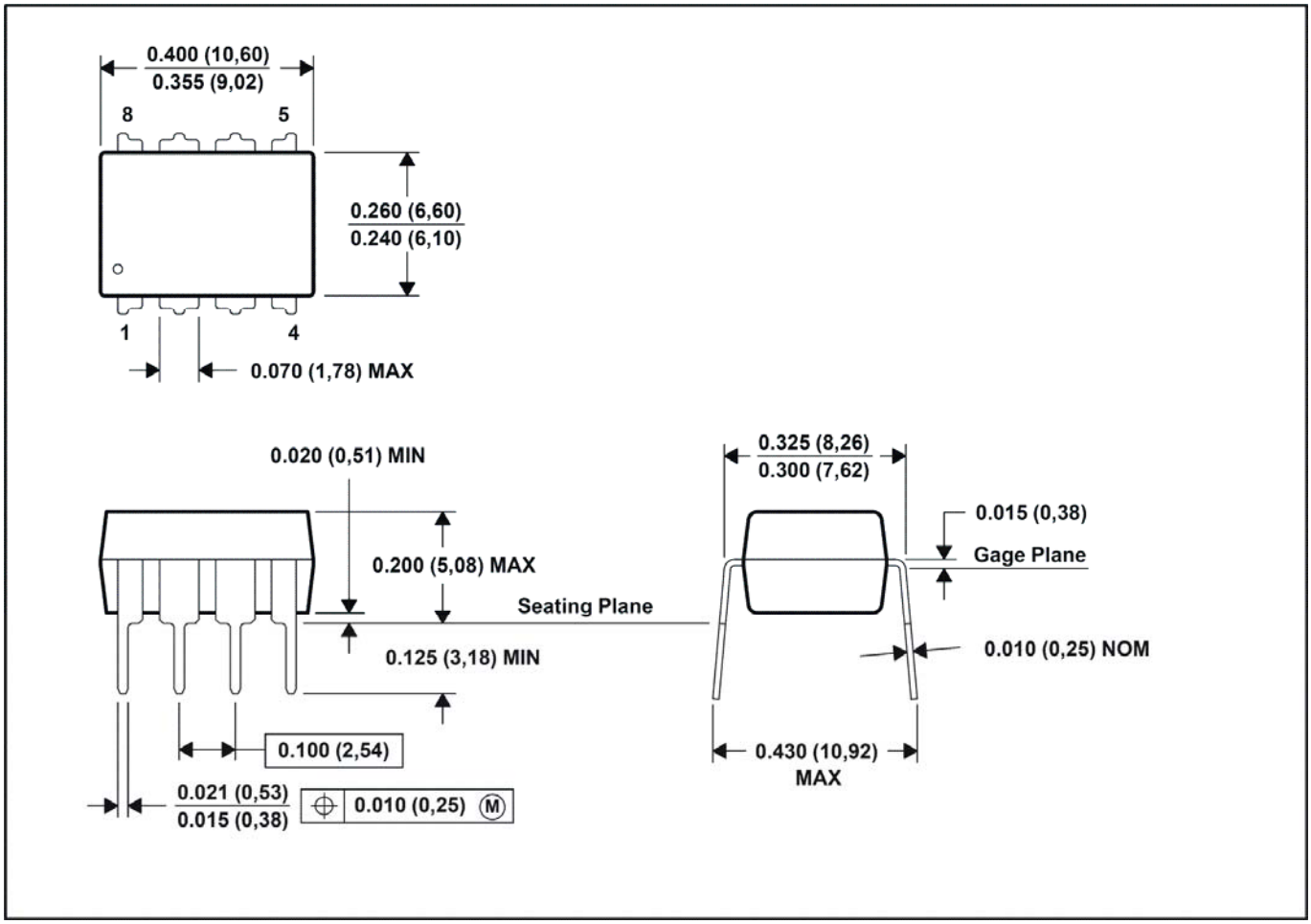
SOP-8 Dimension



NOTES:

A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) per side.
E. Falls within JEDEC MS-012 variation AA.

DIP-8 Dimension



NOTES:

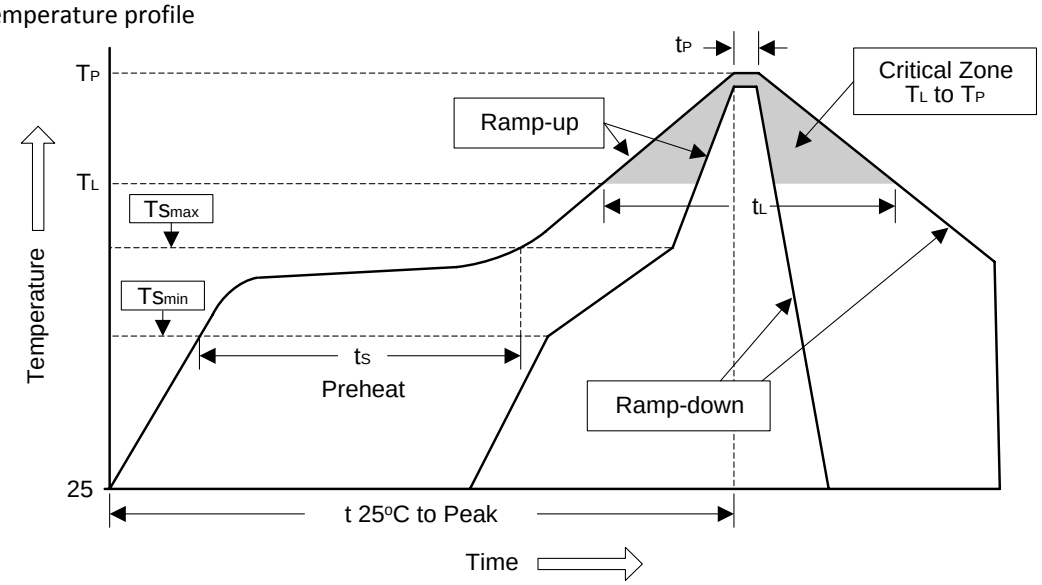
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001.

Soldering Methods for Orister's Products

1. Storage environment: Temperature=10°C~35°C Humidity=65%±15%

2. Reflow soldering of surface-mount devices

Figure 1: Temperature profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (min to max) (ts)	 100°C 150°C 60~120 sec	 150°C 200°C 60~180 sec
Tsmax to T_L - Ramp-up Rate	 <3°C/sec	 <3°C/sec
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60~150 sec	 217°C 60~150 sec
Peak Temperature (T_P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak temperature	Dipping time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

Important Notice: